



# United States Patent and Trademark Office

UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/755,236	01/05/2001	Kenichiro Imai	450100-02940 3751 EXAMINER	
20999 7	7590 07/26/2005			
FROMMER LAWRENCE & HAUG			MANOSKEY, JOSEPH D	
NEW YORK,	VENUE- 10TH FL. NY 10151		ART UNIT	PAPER NUMBER
,		•	2113	
			DATE MAILED: 07/26/2005	

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)				
	09/755,236	IMAI ET AL.				
Office Action Summary	Examiner	Art Unit				
	Joseph D. Manoskey	2113				
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply						
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.  - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.  - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.  - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).						
Status		·				
1) Responsive to communication(s) filed on 17 May 2005.						
2a) ☐ This action is <b>FINAL</b> . 2b) ☑ This	s action is non-final.					
•	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.					
Disposition of Claims						
4) ⊠ Claim(s) 1.6 and 11-14 is/are pending in the application.  4a) Of the above claim(s) is/are withdrawn from consideration.  5) □ Claim(s) is/are allowed.  6) ⊠ Claim(s) 1.6,11 and 13 is/are rejected.  7) ⊠ Claim(s) 12 and 14 is/are objected to.  8) □ Claim(s) are subject to restriction and/or election requirement.						
Application Papers						
9) The specification is objected to by the Examiner.						
10)⊠ The drawing(s) filed on <u>05 January 2001</u> is/are: a)⊠ accepted or b)⊡ objected to by the Examiner.						
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).						
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.						
Priority under 35 U.S.C. § 119						
<ul> <li>12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).</li> <li>a) All b) Some * c) None of:</li> <li>1. Certified copies of the priority documents have been received.</li> <li>2. Certified copies of the priority documents have been received in Application No.</li> <li>3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).</li> <li>* See the attached detailed Office action for a list of the certified copies not received.</li> </ul>						
Attachment(s)						
1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date	4) Interview Summary Paper No(s)/Mail Da 5) Notice of Informal P 6) Other:					

Ke

#### **DETAILED ACTION**

# Claim Rejections - 35 USC § 103

- 1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
  - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 2. Claims 1, 6, 11, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Circello et al, U.S. Patent 5,964,893, hereinafter referred to as "Circello" in view of Fasang, U.S. Patent 4,433,413...
- 3. Referring to claims 1 and 6, Circello teaches a data processing system executing both breakpoint and trace functions in real time, this is interpreted as a monitoring system (See Col. 3, lines 24-30). Circello teaches the system being attached to an external development system, this is interpreted as an external monitoring means for monitoring the state of a controller within an apparatus to be monitored, the state being obtained when a control program stored in storage means in the apparatus controls, via an internal bus of the apparatus, said controller to operate (See Fig. 1 and Col. 3, lines 24-30).

Circello discloses the system, which operates in real time, being monitored containing a debug module that contains an Address Breakpoint High Register (ABHR),

Page 3

an Address Breakpoint Low Register (ABLR), a Data Breakpoint Mask Register (DBMR) and a Data Breakpoint Register) with comparators to compare addresses and data on the bus, thus bus-access detection means, this is interpreted as a bus-access detection means for detecting, in real time, based on internal bus information, each match of an address set with an address line on said internal bus by said controller; said bus-access detection means being external to said controller and internal to said apparatus (See Fig. 1 and 2, Col. 3, lines 24-30, and Col. 5, lines 40-49).

Circello discloses the system, which operates in real time, being monitored containing a debug module that contains a Program Counter Breakpoint Mask Register (PBMR), a Program Counter Breakpoint Register (PBR) and a temporary program counter (PC) register with a comparator to compare the program counter, which is the current executed address of the program running on the processor, thus execution address detection means, this is interpreted as comprising execution address detection means for detecting execution address information of said external monitoring means in real time based on said internal bus information, said execution address means being external to said controller and internal to said apparatus (See Fig. 1 and 2, Col. 3, lines 24-30, and Col. 5, lines 40-49).

Circello discloses the debug module, of the system that operates in real time, being connected to the external development system to send and receiving data, this is interpreted as wherein information on each match and the execution address information are output to said external monitoring means in real time (See Fig. 1 and 2, and Col. 3, lines 24-30).

Application/Control Number: 09/755,236 Page 4

Art Unit: 2113

Circello teaches the system displaying the response to an external user (See Col. 8, lines 34-36). Circello does teach the data being displayed numerically, however Circello does disclose displaying the response to an external user but remains silent about what format the data is displayed in (See Col. 8, lines 34-36). Fasang teaches a device and method of testing a microprocessor system that includes a display where the data is formatted numerically (See Fig. 1, Col. 3, lines 20-31, and Col. 24, lines 5-9). It would have been obvious to one of ordinary skill in the art at the time of the invention to display the data in the numerical format of Fasang on the display of Circello. This would have been obvious to one of ordinary skill in the art at the time of the invention to do this because it better conveys information to the outside world (See Fasang, Col. 3, lines 30-32).

4. Referring to claims 11 and 13, Circello and Fasang teach all the limitations (See rejection of claims 1 and 6 respectively) including wherein said display sets a hold time selected from predetermined values for displaying said information on each match and said execution address information. Fasang teaches leaving the display on long enough for it to be seen and this is accomplished by running a loop for two seconds, this is interpreted as a hold time selected from a predetermined value for displaying (See Col. 24, lines 5-11).

### Allowable Subject Matter

Application/Control Number: 09/755,236 Page 5

Art Unit: 2113

5. Claims 12 and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

# Response to Arguments

6. Applicant's arguments filed 05 April 2005 have been fully considered but they are not persuasive. The Applicant argues that the debug device of Circello can not meet both the bus-access detection means and the execution address detection means because 1) the applicant feels that the cited locations of Circello does not teach both the detection means and 2) the two detection means are physically distinct and perform different functions. The Examiner respectfully disagrees.

Circello teaches the debugger containing a breakpoint registers that serve multiple purposes. Circello teaches an Address Breakpoint High Register (ABHR), an Address Breakpoint Low Register (ABLR), a Data Breakpoint Mask Register (DBMR) and a Data Breakpoint Register) with comparators to compare addresses and data on the bus, thus bus-access detection means. Circello also teaches a Program Counter Breakpoint Mask Register (PBMR), a Program Counter Breakpoint Register (PBR) and a temporary program counter (PC) register with a comparator to compare the program counter, which is the current executed address of the program running on the processor, thus execution address detection means (See Fig. 1 and 2, Col. 3, lines 24-30, and Col. 5, lines 40-49). The above rejections have been amended to include this clarification.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., that the detection means are physically distinct) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Also the mere fact that a given structure is integral does not preclude its consisting of various elements. The Debugger consists of physically distinct breakpoint registers, Address and Data Breakpoint Registers and Program Counter Breakpoint Registers, which are all physically distinct.

### Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Manoskey whose telephone number is (571) 272-3648. The examiner can normally be reached on Mon.-Fri. (7:30am to 4pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Application/Control Number: 09/755,236 Page 7

Art Unit: 2113

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JDM July 20, 2005

ROBERT BEAUSOLIEL
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100